REMARKS

Reconsideration and the timely allowance of the pending claims, in view of the following remarks, are respectfully requested.

In the pending Office Action, the Examiner withdrew the allowance of claims 15-17 and rejected claims 14-15 and 18, under 35 U.S.C. §103(a), as allegedly being unpatentable in view of Nakagawa (Repeater Optical Transmission Experiments with a Highly Sensitive Optical Preamplifier) and Gersbach '405 (U.S. Patent No. 5,293,405); and rejected claims 16-17, under 35 U.S.C. §103(a), as allegedly being unpatentable in view Nakagawa, Gersbach '405, and Phillips '179 (U.S. Patent No. 6,178,179).

By this Amendment, Applicant has amended independent claim 15 to provide a clearer presentation of the claimed subject matter. Applicant submits that no new matter has been introduced. As such, claims 14-18 are presented for examination, of which claim 15 remains the sole independent claim.

Applicant traverses the rejections of claims 14-18, under §103(a), for the following reasons:

As indicated above, independent claim 15, as amended, now positively recites that the processor comprises a decoding mechanism configured to, *inter alia*, split the corrected data signal into component data signals and convert the component data signals into digital component data signals synchronized to a data clock reference signal. The claim also positively recites that the processor comprises an encoding mechanism configured to, *inter alia*, convert the synchronized digital component data signals as output signals, and transmit at least one of the output signals as the regenerated data signal.

There is nothing in the applied references, whether taken alone or in combination, that remotely teach the combination of features recited by claim 15. For example, as acknowledged by the Examiner, the Nakagawa reference fails to teach or

suggest a processor that receives the distorted data signal, regenerates the data signal, and outputs the regenerated data signal – much less a processor that comprises encoding and decoding mechanisms, as required by claim 15.

The Gersbach '405 reference does teach the use of an equalization and regeneration circuit **12**, a peak detect and averaging circuit **14**, and an equalizer control circuit **16**. (*See, e.g.*, Gersbach '405: col. 4, lines 30-37; FIG. 1). The equalization and regeneration circuit **12** is designed to amplify the degraded signal, equalize the amplified and degraded signal by reshaping it, and regenerate the signal in its original form. The peak detect and averaging circuit **14** is configured to control the degree of amplification of the received signal by the equalization and regeneration circuit **12**. The equalizer control circuit **16** is designed to detect and calculate the variances in amplitude and instantaneous frequency degradation of the received signal and uses these variances to control the equalization of the amplified signal. (*See, e.g.*, Gersbach '405: col. 5, lines 17-29; FIG. 1).

There is, however, nothing in the Gersbach '405 reference that remotely teaches the use of a processor including a decoding mechanism that splits the corrected data signal into component data signals and converts the component data signals into digital component data signals synchronized to a data clock reference signal, as required by claim 15. Nor is there anything in Gersbach '405 that teaches the use of a processor including an encoding mechanism that converts the synchronized digital component data signals as output signals, and transmits at least one of the output signals as the regenerated data signal, as also required by claim 15.

The Phillips '179 reference does nothing to cure the deficiencies noted above regarding the Nakagawa and Gersbach '405 references. That is, Phillips '179 merely mentions the use of signal regenerator **28**, located between the central office and customer locations, to extend the distribution range by decoding signals traveling in either direction so that the signals can be retransmitted at original signal quality and strength. (*See, e.g.*, Phillips '179: col. 3, lines 12-17; FIG. 1). Phillips '179 also identifies the use of a translator unit **34**, located between the central office and

customer locations, for providing multiple code compatibility to repackage the data into a different format. The translator unit **34** includes a receiver **36** for receiving signals, a decoder **38** for analog-to-digital conversion and decoding the IP-encapsulated ATM payload data from the received signal, and a buffer **40** for temporarily storing the base data. (*See, e.g.*, Phillips '179: col. 3, lines 48-55; FIG. 1).

As such, the Phillips '179 reference is clearly devoid of teaching a processor that includes a decoding mechanism that splits the corrected data signal into component data signals and converts the component data signals into digital component data signals synchronized to a data clock reference signal, as required by claim 15. Nor is Phillips '179 capable of teaching the use of a processor that includes an encoding mechanism that converts the synchronized digital component data signals as output signals, and transmits at least one of the output signals as the regenerated data signal, as also required by claim 15.

For at least these reasons, Applicant submits that none of the references, either alone or in combination, teach the combination of features recited by claim 15. Accordingly, claim 15 is patentable over these references. Moreover, claims 14 and 16-18, which depend from claim 15 are also patentable by virtue of dependency as well as for their additional recitations. Thus, Applicant requests the immediate withdrawal of the §103(a) rejections of claims 14–18.

All matters having been addressed, Applicant respectfully requests the entry of this Amendment, the Examiner's reconsideration of this application, and the immediate issuance of a Notice of Allowance indicating that claims 14-18 are finally allowed.

Applicant's Counsel remains ready to assist the Examiner in any way to facilitate and expedite the prosecution of this application.

Please charge any fees associated with the submission of this paper to Deposit Account Number **033975**. The Commissioner for Patents is also authorized to credit any over payments to the above-referenced Deposit Account.

Respectfully submitted,

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